IP-UNIV-SERIAL

Dual Channel
High Speed Serial
IndustryPack

User Manual

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Dual Channel
High Speed Serial
IndustryPack

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Product Description

The IP-UNIV-SERIAL is part of the IndustryPack® family of modular I/O components. It is an upgrade to the IP-Serial. The pin assignments and basic features remain essentially the same but the address map and register formats have changed. IP-UNIV-SERIAL provides internal data buffering, data rates up to 10 megabits per second, and support for nearly all serial protocols. The IP-UNIV-SERIAL incorporates the Zilog Z16C30 Universal Serial Controller (USC) which includes 32 byte FIFO buffers for both transmit and receive data on each of the two independent channels. Protocols supported by the Z16C30 include HDLC, SDLC, Bisync, NRZ, NRZI, and Biphase. Additional capabilities include 16 and 32-bit CRC generation and checking, one to eight bits per character, one address/data bit, MIL STD 1553B protocol support, sync stripping, preamble generation, and digital phase-locked loop circuits for clock recovery. The USC provides a flexible bus interface architecture that is configured by the first write to the device, refer to the Zilog documentation for details on Z16C30 programming.

The IP-UNIV-SERIAL includes an on board 3.6864 MHz oscillator that can be prescaled with the Z16C30 to create all of the standard baud rates. A separate socket is provided for a user oscillator. A single external clock interface is provided so that the IP-UNIV-SERIAL can either operate from an external reference clock or provide an external reference clock.

Channel A and Channel B within the USC device are almost completely independent. Each channel has a complete prescaler, vector register, interrupt controller, and protocol controller. Both channels share the external clock interface. Refer to the Zilog documentation for details on the Z16C30.

Independent interrupt vectors and controls are provided for each IP-UNIV-SERIAL channel. Channel A is given priority over Channel B in the event of simultaneous interrupt requests. If Channel B asserts an interrupt request before Channel A, then the Channel A interrupt request will be held off until the Channel B interrupt is acknowledged. Interrupt priority and sequencing is controlled by a programmable device. Please contact SBS if your application has special requirements.

The RS-232, RS-422, and RS-485 compatible interface circuit facilitates interfacing with a wide variety of equipment. Three SIP resistor packs are used to configure the electrical characteristics of the serial I/O interface. RP3 is a pull-up package used to control the current available to the “reference” pin of the receivers during single ended operation. During RS-232 operation the ‘+’ side of the differential receivers is set to approximately 3 volts. The minus side is used as the RS-232 input. RP1 and RP2 are packaged discrete resistors used as terminating resistors for differential operation. The standard IP is supplied with a nominal resistance of 100Ω. The user may select and install alternate SIP resistors to optimize the termination for the application. RP1 and RP2 should not be installed for single ended configurations to prevent the drive voltage from being applied to the reference pin. RP3 should not be installed during differential operation. However; in most cases, the small current drain added by RP3 will not result in improper operation.

Serial Interface	Resistor Packs Installed	Resistor Packs Removed
RS-232	RP3 (2KΩ)	RP1 and RP2 (100Ω)
RS-422	RP1 and RP2 (100Ω)	RP3 (2KΩ)
RS-485	RP1 and RP2 (100Ω)	RP3 (2KΩ)

Figure 1 IP-UNIV-SERIAL Resistor Pack Configuration

A block diagram of the IP-UNIV-SERIAL is shown below in Figure 2.

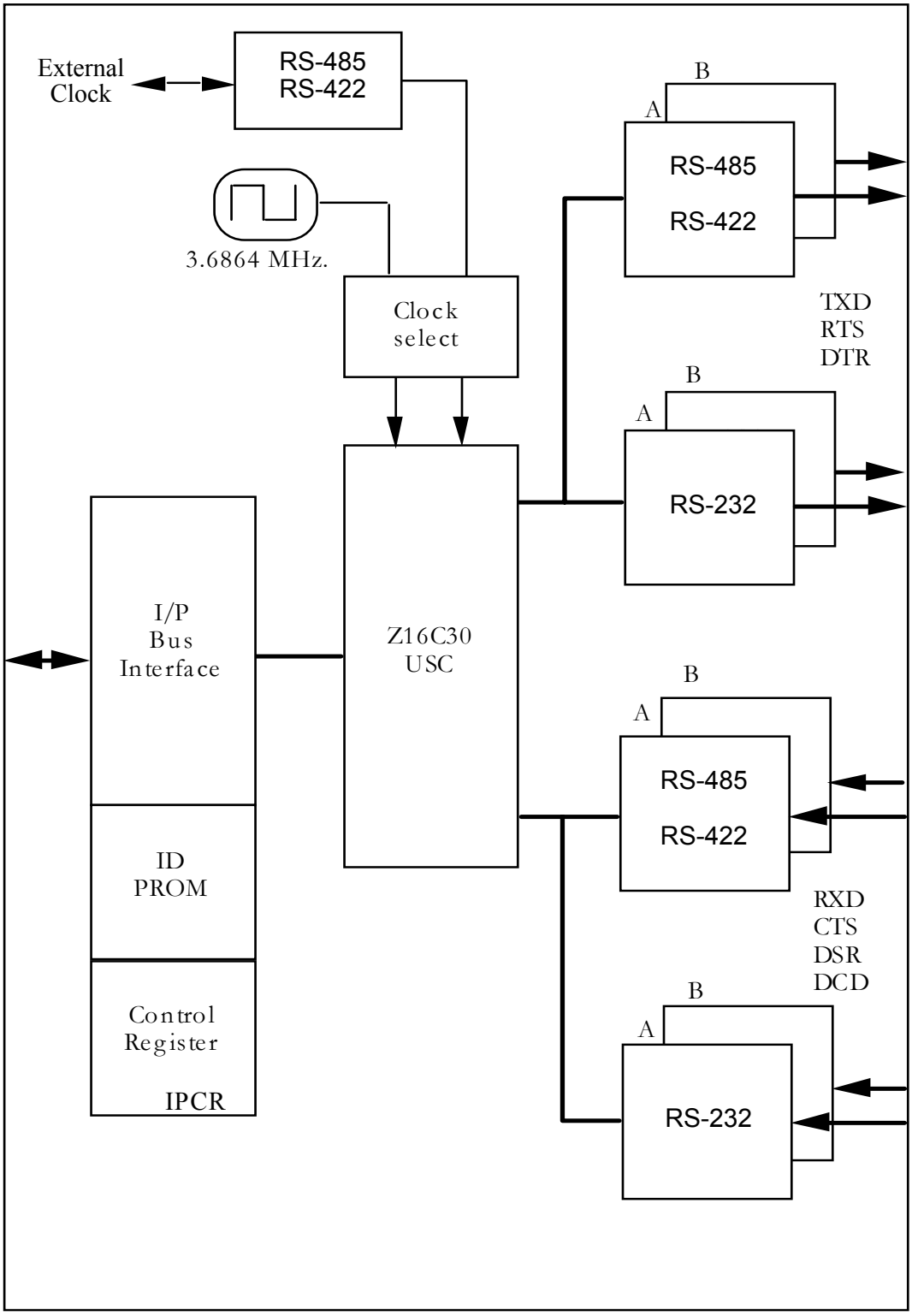

Figure 2 IP-UNIV-SERIAL Block Diagram

VMEbus Addressing

The address map of the IP-UNIV-SERIAL on the VMEbus is given in Figures 3 and 4 below. All registers are accessed in IP I/O space. The Receive/Transmit Data Register can be accessed as either a word or a byte. All other registers on the IP-UNIV-SERIAL are word registers. Byte accesses are on data lines D7..D0. Word access are on data lines D15..D0.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

Register Name	68K Address	Access
Channel Command/Address Register (CCAR_B)	$00	Word, R/W
Channel Mode Register (CMR_B)	$02	Word, R/W
Channel Command/Status Register (CCSR_B)	$04	Word, R/W
Channel Control Register (CCR_B)	$06	Word, R/W
Bus Configuration Register [first write only] (BCR)	$08	Word, W
IndustryPack Control Register (IPCR)	$0A	Word, R/W
Test Mode Data Register (TMDR_B)	$0C	Word, R/W
Test Mode Control Register (TMCR_B)	$0E	Word, R/W
Clock Mode Control Register (CMCR_B)	$10	Word, R/W
Hardware Configuration Register (HCR_B)	$12	Word, R/W
Interrupt Vector Register (IVR_B)	$14	Word, R/W
I/O Control Register (IOCR_B)	$16	Word, R/W
Interrupt Control Register (ICR_B)	$18	Word, R/W
Daisy-Chain Control Register (DCCR_B)	$1A	Word, R/W
Misc. Interrupt Status Register (MISR_B)	$1C	Word, R/W
Status Interrupt Control (SICR_B)	$1E	Word, R/W
Receive/Transmit Data Register (RDR/TDR_B)	$20	Word, R/W
Receive/Transmit Data Register (RDR/TDR_B)	$21	Byte, R/W
Receive Mode Register (RMR_B)	$22	Word, R/W
Receive Command/Status Register (RCSR_B)	$24	Word, R/W
Receive Interrupt Control Register (RICR_B)	$26	Word, R/W
Receive Sync Register (RSR_B)	$28	Word, R/W
Receive Count Limit Register (RCLR_B)	$2A	Word, R/W
Receive Character Count Register (RCCR_B)	$2C	Word, R/W
Time Constant 0 Register (TC0R_B)	$2E	Word, R/W
Alias of address $20	$30	Word, R/W
Transmit Mode Register (TMR_B)	$32	Word, R/W
Transmit Command/Status Register (TCSR_B)	$34	Word, R/W
Transmit Interrupt Control Register (TICR_B)	$36	Word, R/W
Transmit Sync Register (TSR_B)	$38	Word, R/W
Transmit Count Limit Register (TCLR_B)	$3A	Word, R/W
Transmit Character Count Register (TCCR_B)	$3C	Word, R/W
Transmit Constant 1 Register (TC1R_B)	$3E	Word, R/W

Figure 3 VMEbus Address Map (Channel B)

See Programming section below and Zilog documentation for register definition details.

All registers are accessed in IP I/O space. The Receive/Transmit Data Register can be accessed as either a word or a byte. All other registers on the IP-UNIV-SERIAL are word registers. Byte accesses are on data lines D7..D0. Word access are on data lines D15..D0.

Register Name	68K Address	Access
Channel Command/Address Register (CCAR_A)	$40	Word, R/W
Channel Mode Register (CMR_A)	$42	Word, R/W
Channel Command/Status Register (CCSR_A)	$44	Word, R/W
Channel Control Register (CCR_A)	$46	Word, R/W
Spare Address, No Register	$48	Word, R/W
Spare Address, No Register	$4A	Word, R/W
Test Mode Data Register (TMDR_A)	$4C	Word, R/W
Test Mode Control Register (TMCR_A)	$4E	Word, R/W
Clock Mode Control Register (CMCR_A)	$50	Word, R/W
Hardware Configuration Register (HCR_A)	$52	Word, R/W
Interrupt Vector Register (IVR_A)	$54	Word, R/W
I/O Control Register (IOCR_A)	$56	Word, R/W
Interrupt Control Register (ICR_A)	$58	Word, R/W
Daisy-Chain Control Register (DCCR_A)	$5A	Word, R/W
Misc. Interrupt Status Register (MISR_A)	$5C	Word, R/W
Status Interrupt Control (SICR_A)	$5E	Word, R/W
Receive/Transmit Data Register (RDR/TDR_A)	$60	Word, R/W
Receive/Transmit Data Register (RDR/TDR_A)	$61	Byte, R/W
Receive Mode Register (RMR_A)	$62	Word, R/W
Receive Command/Status Register (RCSR_A)	$64	Word, R/W
Receive Interrupt Control Register (RICR_A)	$66	Word, R/W
Receive Sync Register (RSR_A)	$68	Word, R/W
Receive Count Limit Register (RCLR_A)	$6A	Word, R/W
Receive Character Count Register (RCCR_A)	$6C	Word, R/W
Time Constant 0 Register (TC0R_A)	$6E	Word, R/W
Alias of address $60	$70	Word, R/W
Transmit Mode Register (TMR_A)	$72	Word, R/W
Transmit Command/Status Register (TCSR_A)	$74	Word, R/W
Transmit Interrupt Control Register (TICR_A)	$76	Word, R/W
Transmit Sync Register (TSR_A)	$78	Word, R/W
Transmit Count Limit Register (TCLR_A)	$7A	Word, R/W
Transmit Character Count Register (TCCR_A)	$7C	Word, R/W
Transmit Constant 1 Register (TC1R_A)	$7E	Word, R/W

Figure 4 VMEbus Address Map (Channel A)

See Programming section below and Zilog documentation for register definition details.

NuBus Addressing

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

NuBus byte address = (VMEbus byte address * 2) – 1

All byte data is still transferred on data lines D7..D0.

Word addresses on the NuBus are the same as for VME. Word data is transferred on data lines D15..D0.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

ISA (PC-AT) Bus Addressing

The address map of the IP-UNIV-SERIAL on the ISA bus is given in Figures 5 and 6 below. All registers are accessed in IP I/O space. The Receive/Transmit Data Register can be accessed as either a word or a byte. All other registers on the IP-UNIV-SERIAL are word registers. Byte accesses are on data lines D7..D0. This byte is the even byte in Intel family host architectures, and the odd byte in Motorola 68K host architectures. Word accesses are on data lines D15..D0.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

Register Name	68K Address	Access
Channel Command/Address Register (CCAR_B)	$00	Word, R/W
Channel Mode Register (CMR_B)	$02	Word, R/W
Channel Command/Status Register (CCSR_B)	$04	Word, R/W
Channel Control Register (CCR_B)	$06	Word, R/W
Bus Configuration Register [first write only] (BCR)	$08	Word, W
IndustryPack Control Register (IPCR)	$0A	Word, R/W
Test Mode Data Register (TMDR_B)	$0C	Word, R/W
Test Mode Control Register (TMCR_B)	$0E	Word, R/W
Clock Mode Control Register (CMCR_B)	$10	Word, R/W
Hardware Configuration Register (HCR_B)	$12	Word, R/W
Interrupt Vector Register (IVR_B)	$14	Word, R/W
I/O Control Register (IOCR_B)	$16	Word, R/W
Interrupt Control Register (ICR_B)	$18	Word, R/W
Daisy-Chain Control Register (DCCR_B)	$1A	Word, R/W
Misc. Interrupt Status Register (MISR_B)	$1C	Word, R/W
Status Interrupt Control (SICR_B)	$1E	Word, R/W
Receive/Transmit Data Register (RDR/TDR_B)	$20	Word, R/W
Receive/Transmit Data Register (RDR/TDR_B)	$20	Byte, R/W
Receive Mode Register (RMR_B)	$22	Word, R/W
Receive Command/Status Register (RCSR_B)	$24	Word, R/W
Receive Interrupt Control Register (RICR_B)	$26	Word, R/W
Receive Sync Register (RSR_B)	$28	Word, R/W
Receive Count Limit Register (RCLR_B)	$2A	Word, R/W
Receive Character Count Register (RCCR_B)	$2C	Word, R/W
Time Constant 0 Register (TC0R_B)	$2E	Word, R/W
Alias of address $20	$30	Word, R/W
Transmit Mode Register (TMR_B)	$32	Word, R/W
Transmit Command/Status Register (TCSR_B)	$34	Word, R/W
Transmit Interrupt Control Register (TICR_B)	$36	Word, R/W
Transmit Sync Register (TSR_B)	$38	Word, R/W
Transmit Count Limit Register (TCLR_B)	$3A	Word, R/W
Transmit Character Count Register (TCCR_B)	$3C	Word, R/W
Transmit Constant 1 Register (TC1R_B)	$3E	Word, R/W

Figure 5 ISA bus Address Map (Channel B)

See Programming section below and Zilog documentation for register definition details.

All registers are accessed in IP I/O space. The Receive/Transmit Data Register can be accessed as either a word or a byte. All other registers on the IP-UNIV-SERIAL are word registers. Byte accesses are on data lines D7..D0. This byte is the even byte in Intel family host architectures, and the odd byte in Motorola 68K host architectures. Word accesses are on data lines D15..D0.

Register Name	68K Address	Access
Channel Command/Address Register (CCAR_A)	$40	Word, R/W
Channel Mode Register (CMR_A)	$42	Word, R/W
Channel Command/Status Register (CCSR_A)	$44	Word, R/W
Channel Control Register (CCR_A)	$46	Word, R/W
Spare Address, No Register	$48	Word, R/W
Spare Address, No Register	$4A	Word, R/W
Test Mode Data Register (TMDR_A)	$4C	Word, R/W
Test Mode Control Register (TMCR_A)	$4E	Word, R/W
Clock Mode Control Register (CMCR_A)	$50	Word, R/W
Hardware Configuration Register (HCR_A)	$52	Word, R/W
Interrupt Vector Register (IVR_A)	$54	Word, R/W
I/O Control Register (IOCR_A)	$56	Word, R/W
Interrupt Control Register (ICR_A)	$58	Word, R/W
Daisy-Chain Control Register (DCCR_A)	$5A	Word, R/W
Misc. Interrupt Status Register (MISR_A)	$5C	Word, R/W
Status Interrupt Control (SICR_A)	$5E	Word, R/W
Receive/Transmit Data Register (RDR/TDR_A)	$60	Word, R/W
Receive/Transmit Data Register (RDR/TDR_B)	$60	Byte, R/W
Receive Mode Register (RMR_A)	$62	Word, R/W
Receive Command/Status Register (RCSR_A)	$64	Word, R/W
Receive Interrupt Control Register (RICR_A)	$66	Word, R/W
Receive Sync Register (RSR_A)	$68	Word, R/W
Receive Count Limit Register (RCLR_A)	$6A	Word, R/W
Receive Character Count Register (RCCR_A)	$6C	Word, R/W
Time Constant 0 Register (TC0R_A)	$6E	Word, R/W
Alias of address $60	$70	Word, R/W
Transmit Mode Register (TMR_A)	$72	Word, R/W
Transmit Command/Status Register (TCSR_A)	$74	Word, R/W
Transmit Interrupt Control Register (TICR_A)	$76	Word, R/W
Transmit Sync Register (TSR_A)	$78	Word, R/W
Transmit Count Limit Register (TCLR_A)	$7A	Word, R/W
Transmit Character Count Register (TCCR_A)	$7C	Word, R/W
Transmit Constant 1 Register (TC1R_A)	$7E	Word, R/W

Figure 6 ISA bus Address Map (Channel A)

See Programming section below and Zilog documentation for register definition details.

Programming

General

The phrase “Logic Interface” refers to the Electrical/Logical interface between an Industry Pack board like the IP-UNIV-SERIAL and the carrier board on which it is installed.

The phrase “I/O Interface” refers to the I/O connector on the Industry Pack that carries the serial I/O signals between the Industry Pack and the carrier board.

The Channel A interrupt request is presented to the IP carrier on IRQ0 of the Logic Interface. The interrupt request from Channel B is presented on IRQ1.

Register Definitions

Refer to the Zilog Z16C30 documentation for specific information about all of the registers and ports in the IP-UNIV-SERIAL register map except for the IndustryPack Control Register (IPCR). The IPCR is a special register that is outside the Z16C30. This register occupies an unused address in the Z16C30 register map. The control lines to the USC are not activated for accesses to the IPCR.

Bus Configuration Register (BCR)

The Bus Configuration Register is used to select the basic hardware interface protocol to be used to access the Zilog Z16C30. A write to the BCR must be the first write to the device after a reset has occurred. Writing a ‘5’ to this register will put the USC into multiplexed mode with 16 bit data and right shifted addresses. This is the recommended configuration.

IndustryPack Control Register (IPCR)

Data Bit	15	14	13	12	11	10	9	8
Rd / Wrt	-	-	-	-	-	-	-	-

Data Bit	7	6	5	4	3	2	1	0
Rd / Wrt	CLKI	CLKO	B485	B422	A485	A422	Unus	RST

Figure 7 IndustryPack Control Register

The IPCR controls the I/O enables and master reset of the USC. Only the least significant eight bits of this register are used. Data written to the most significant eight bits is ignored and data read from these bits is undefined. The initial value of the IPCR after a hardware reset is $FF.

Bit [0] S/W Reset [R/W]
The S/W Reset bit is “anded” with the system reset and driven to the USC. Power-up reset and S/W reset have the same affect. Bit 0 should be set low and then returned high to create a reset pulse. The reset signal must be low for 170 nanoseconds and high for 70 nanoseconds before the next access involving the USC is made. With the timing constraints of the IP Interface back-to-back instructions can be used to create the reset pulse. Note that the USC will not respond to CPU accesses while reset is low.

Bit [1] Unused [R/W]
Bit 1 of the IPCR is not used on the IP but is supported by a latch. Data written to this bit is stored in the register and made available when the IPCR is read.

Bit [2] Channel A RS-422 (RS-232) Enable [R/W]
When a '0' is written to Bit 2 the Channel A RS-422 receivers are enabled. The RS-422 receivers are also used as RS-232 receivers. The configuration of the resistor packs to support either RS-422 or RS-232 mode is described in the Product Description section. It is possible to create hardware conflicts with improper enable selection. For example, IPCR bits 2 and 3 must never both be '0' at the same time. If both of these bits are '0' then the Channel A receive data input of the USC (RxDA) will have two sources.

Bit [3] Channel A RS-485 Enable [R/W]
When a '0' is written to Bit 3 the Channel A RS-485 receivers are enabled. It is possible to create hardware conflicts with improper enable selection. For example, IPCR bits 2 and 3 must never both be '0' at the same time. If both of these bits are '0' then the Channel A receive data input of the USC (RxDA) will have two sources.

Configuration	Bits 3 and 2	
Reset	1	1
RS-232 or RS-422	1	0
RS-485	0	1
INVALID	**0**	**0**

Figure 8 Channel A Receiver Controls

Bit [4] Channel B RS-422 (RS-232) Enable [R/W]
When a '0' is written to Bit 4 the Channel B RS-422 receivers are enabled. The RS-422 receivers are also used as RS-232 receivers. The configuration of the resistor packs to support either RS-422 or RS-232 mode is described in the Product Description section. It is possible to create hardware conflicts with improper enable selection. For example, IPCR bits 4 and 5 must never both be '0' at the same time. If both of these bits are '0' then the Channel B receive data input of the USC (RxDB) will have two sources.

Bit [5] Channel B RS-485 Enable [R/W]
When a '0' is written to Bit 5 the Channel B RS-485 receivers are enabled. It is possible to create hardware conflicts with improper enable selection. For example, IPCR bits 4 and 5 must never both be '0' at the same time. If both of these bits are '0' then the Channel B receive data input of the USC (RxDB) will have two sources.

Configuration	Bits 5 and 4	
Reset	1	1
RS-232 or RS-422	1	0
RS-485	0	1
INVALID	**0**	**0**

Figure 9 Channel B Receiver Controls

Bit [6] Reference Clock Output Enable [R/W]
The IP-UNIV-SERIAL supports a Reference Clock channel that can be either an input or output. This clock can be either single ended or differential. Writing a '1' to Bit 6 enables the Reference Clock driver. The Reference Clock Output Enable and Reference Clock Input Enable are set to enable Reference Clock Output by power on reset. The Reference Clock channel is driven from or received through the RxC pins of the Z16C30. The CCR, HCR, IOCR, CMR, and CMCR can be coordinated to create the desired clock rate as an output or to select the clock signal as a controlling input. Refer to the Zilog documentation for bit map definitions of the various registers.

Bit [7] Reference Clock Input Enable [R/W]
The IP-UNIV-SERIAL supports a Reference Clock channel that can be either an input or output. This clock can be either single ended or differential. Writing a '0' to Bit 7 enables the Reference Clock receiver. The Reference Clock Output Enable and Reference Clock Input Enable are set to disable Reference Clock Input by power on reset. The Reference Clock channel is driven from or received through the RxC pins of the Z16C30. The CCR, HCR, IOCR, CMR, and CMCR can be coordinated to create the desired clock rate as an output or to select the clock signal as a controlling input. Refer to the Zilog documentation for bit map definitions of the various registers.

Configuration	Bits 7 and 6	
Drive External Clock	1	1
Disable External Clock	1	0
INVALID	**0**	**1**
Receive External Clock	0	0

Figure 10 External Clock Interface Controls

IP-UNIV-SERIAL Configuration			IPCR Data (hex)
Software Reset			$FFFE
Clear Software Reset			$FFFF
No External Clock	Channel B–RS-232/RS-422	Channel A–RS-232/RS-422	$FFAB
No External Clock	Channel B–RS-232/RS-422	Channel A–RS-485	$FFA7
No External Clock	Channel B–RS-485	Channel A–RS-232/RS-422	$FF9B
No External Clock	Channel B–RS-485	Channel A–RS-485	$FF97
External Clock Out	Channel B–RS-232/RS-422	Channel A–RS-232/RS-422	$FFEB
External Clock Out	Channel B–RS-232/RS-422	Channel A–RS-485	$FFE7
External Clock Out	Channel B–RS-485	Channel A–RS-232/RS-422	$FFDB
External Clock Out	Channel B–RS-485	Channel A–RS-485	$FFD7
External Clock In	Channel B–RS-232/RS-422	Channel A–RS-232/RS-422	$FF2B
External Clock In	Channel B–RS-232/RS-422	Channel A–RS-485	$FF27
External Clock In	Channel B–RS-485	Channel A–RS-232/RS-422	$FF1B
External Clock In	Channel B–RS-485	Channel A–RS-485	$FF17

Figure 11 Valid IPCR Configurations

Transmission Line Driver Enables

The RS-232 drivers on the single ended Transmit Data, Request To Send and Data Terminal Ready lines are always enabled. The single ended and differential transmission signals are routed to separate I/O Interface pins.

Several pins on the Z16C30 can be used for general I/O or DMA handshake signals. On the IP-UNIV-SERIAL these pins are used as general I/O. The Receive Request (RxREQ) pin of each channel is used to control the RS-485/RS-422 drivers on the differential Request To Send and Data Terminal Ready lines. The RxREQ pin must be programmed to output a '1' to enable the drivers. Programming the RxREQ pin to output a '0' disables the drivers. The Zilog documentation contains details on programming the I/O Control Register bits in the USC that controls the RxREQ pin.

In a similar manner, the Receive Acknowledge (RxACK) pin of each channel is used to control the RS-485/RS-422 driver on the differential Transmit Data line of that channel. The RxACK pin must be programmed to output a '1' to enable the drivers. Programming the RxACK pin to output a '0' disables the drivers. Refer to the Zilog documentation for details on programming the Hardware Configuration Register bits in the USC that controls the RxACK pin.

The transmission driver enables can not create internal conflicts on the IP but may be able to create external conflicts depending on your system. Most of the transmission drivers are enabled on power-up while all of the receivers are disabled. Undesired differential transmission drivers can be disabled as a part of the power-on initialization sequence.

Z16C30 Pin	State	Z16C30 Register	RS-422 Drivers Enabled
RxREQ	Output 1	I/O Control	RTS and DTR
RxACK	Output 1	Hardware Config.	TxD

Figure 12 Transmission Line Driver Controls

Modem Control Signals

The Clear To Send (CTS) and Data Carrier Detect (DCD) pins of the Z16C30 can be used as a transmitter enable (CTS) and as a receiver enable (DCD). The DCD pin can be used as a Data Set Ready (DSR) pin in those applications where DSR is substituted for DCD. These pins can also be programmed for use as general I/O. On the IP-UNIV-SERIAL the remaining DMA handshake pins Transmit Request (TxREQ) and Transmit Acknowledge (TxACK) are wired to drivers to support Data Terminal Ready (DTR) and Request To Send (RTS). The TxREQ pin is wired to the DTR drivers. The TxACK pin is wired to the RTS drivers. Refer to the Zilog documentation for details on programming the I/O Control Register bits in the USC that controls the CTS, DCD, TxREQ and RxREQ pins. The TxACK pin control is contained in the Hardware Configuration Register. The I/O Control Register contains the controls for the CTS, DCD and TxREQ pins.

Z16C30 Pin	Z16C30 Register	Modem Control Signals
TxREQ	I/O Control	DTR
TxACK	Hardware Config.	RTS
CTS	I/O Control	CTS
DCD	I/O Control	DCD / DSR

Figure 13 Modem Controls

Universal Serial Sample Test Configuration

The following series of register accesses to an IP-UNIV-SERIAL will allow the user to output ASCII characters at 9600 bps from pin 3 of the IP I/O interface. This can be observed with an oscilloscope, logic probe, or lighted break-out box.

The base address of the IndustryPack I/O Space should be added to the addresses given in the table below when using the debugger to write the values. This is commonly $FF6000 for Pack A of the VIPC310 Carrier Board, and is $FFF58000 for Pack A of the Motorola MVME162.

All values in the table below are hexadecimal, and should be written using WORD (16-bit) accesses.

Note that for proper RS-232 operation, resistor packs RP1 and RP2 should be removed from the IP-UNIV-SERIAL prior to its installation in the carrier board.

Register	Offset	Value
IPCR	$0A	$00A9
BCR	$08	$0005
CCAR	$40	$0400
CCAR	$40	$0000
CMCR	$50	$0324
HCR	$52	$0001
TC0R	$6E	$0017
RMR	$62	$0002
TMR	$72	$0002

Figure 14 IndustryPack Control Register Values for Testing

Characters may now be written to the Transmit Data Register for conversion to serial. Word writes to offset $60 will result in the transmission of two characters, while byte writes to offset $61 will result in the transmission of a single character.

ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision IP, it may check for it directly.

Standard data in the ID PROM on the IP-UNIV-SERIAL is shown in Figure 15 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification. The ID PROM on the IP-UNIV-SERIAL is implemented using an 82S123 20-pin surface mount device.

The location of the ID PROM in the host's address space is dependent on the carrier used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F 19	(available for user)	
17	CRC for bytes used	(8A)
15	No of bytes used	(0C)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(00)
0F	reserved	(00)
0D	Revision	(C1)
0B	Model No IP-UNIV-SERIAL	(45)
09	Manufacturer ID SBS	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 15 ID PROM Data (hex)

I/O Pin Wiring

This section lists the I/O Interface pin assignments for IP-UNIV-SERIAL.

The pin numbers given in Figures 16 and 17 below correspond to numbers on the 50-pin IndustryPack I/O connector (P2), to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

Flat Cable Channel A	D-Shell	I/O	RS-232 Signal	RS-422/RS-485 Signal
1	1		GND	GND
3	2	O	TxD	
5	3	I	RxD	RxD-
7	4	O	RTS	
9	5	I	CTS	CTS+
11	6	I	Do Not Connect	DSR-/DCD-
13	7		GND	GND
15	8	I	DSR/DCD	DSR+/DCD+
17	9	O		TxD+
19	10			GND
21	11	I/O		Rx_Tx_C+
23	12			GND
25	13	I		CTS-
2	14	O		DTR-
4	15			GND
6	16	I		RxD+
8	17	O		DTR+
10	18	O		RTS+
12	19	O		RTS-
14	20	O	DTR	
16	21			GND
18	22	O		TxD-
20	23	I/O		Rx_Tx_C-
22	24			GND
24	25			Fused +5V

Figure 16 I/O Pin Definitions (Channel A)

When operating Channel A of the IP-UNIV-SERIAL in RS-232 mode make no connection to pin 11 of the IndustryPack I/O connector (P2). Connecting an RS-232 signal, such as DSR, to this pin will cause corruption of the DCD signal on pin 15 of the IndustryPack I/O connector (P2). Similarly, when operating Channel B of the IP-UNIV-SERIAL in RS-232 mode make no connection to pin 36 of the IndustryPack I/O connector (P2). Connecting an RS-232 signal, such as DSR, to this pin will cause corruption of the DCD signal on pin 40 of the IndustryPack I/O connector (P2).

Flat Cable Channel B	D-Shell	I/O	RS-232 Signal	RS-422/RS-485 Signal
26	1		GND	GND
28	2	O	TxD	
30	3	I	RxD	RxD-
32	4	O	RTS	
34	5	I	CTS	CTS+
36	6	I	Do Not Connect	DSR-/DCD-
38	7		GND	GND
40	8	I	DSR/DCD	DSR+/DCD+
42	9	O		TxD+
44	10			GND
46	11			
48	12			GND
50	13	I		CTS-
27	14	O		DTR-
29	15			GND
31	16	I		RxD+
33	17	O		DTR+
35	18	O		RTS+
37	19	O		RTS-
39	20	O	DTR	
41	21			GND
43	22	O		TxD-
45	23			
47	24			GND
49	25			Fused +5V

Figure 17 I/O Pin Definitions (Channel B)

Signals have been assigned to the RS-422/RS-485 driver and receiver pins to maintain the same signal phasing found in the RS-232 interface. For example, CTS+ is connected to the negative input pin of the receiver and CTS- is connected to the positive input of the receiver to produce an active low, negative true, Clear To Send at the input to the Z16C30.

The IP-UNIV-SERIAL supports RS-485 bi-directional, multipoint, operation on the TxD+ and TxD– pins. Refer to the Programming section earlier in this manual for details on controlling the transceiver.

The bi-directional External Reference Clock (Rx_Tx_C) is only available as part of the Channel A interface. The corresponding pins of the Channel B interface are unused. The Receive Clock (RxC) pins of both channels are tied to the External Reference Clock interface and User Oscillator circuit.

IndustryPack Logic Interface Pin Assignment

Figure 18 below gives the pin assignments for the IndustryPack Logic Interface on the IP-UNIV-SERIAL. Pins marked n/c below are defined by the specification, but are not used on IP-UNIV-SERIAL. Also see the User Manual for your IP Carrier board for more information.

GND	GND	1		26	
CLK	+5V		2		27
Reset*	R/W*	3		28	
D0 IDSel*	4		29		
D1 n/c	5	30			
D2 MEMSel*	6		31		
D3 n/c	7	32			
D4 INTSel*	8		33		
D5 n/c	9	34			
D6 IOSel*	10		35		
D7 n/c	11	36			
D8 A1	12		37		
D9 n/c	13	38			
D10	A2	14		39	
D11	n/c 15		40		
D12	A3	16		41	
D13	IntReq0*	17		42	
D14	A4	18		43	
D15	IntReq1*	19		44	
BS0*	A5	20		45	
BS1*	n/c 21		46		
–12V	A6	22		47	
+12V	Ack*	23		48	
+5V	n/c	24		49	
GND	GND	25		50	

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 18 Logic Interface Pin Assignment

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-UNIV-SERIAL is constructed out of 0.062 inch thick FR4 V0 material. The four copper layers consist of two signal layers on the top and bottom, and two internal layers dedicated to power and ground planes.

Through hole and surface mounting of components is used. IC sockets use gold plated screw-machine pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold plated on both plugs and receptacles. The pins are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four stainless steel M2 metric screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Repair

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS Technologies will not be responsible for damages due to improper packaging of returned items. For service SBS Technologies products not purchased directly from SBS Technologies, contact your reseller. Products returned to SBS Technologies for repair by other than the original customer will be treated as out-of-warranty.

Specifications IP-UNIV-SERIAL

This section gives the technical specification for the standard grade IP-UNIV-SERIAL.

Number of Channels:	Two serial channels Up to 10 Mbit/sec data rate Address/data bit support 16 or 32 bit CRC generation/checking Low power CMOS
I/O Interface:	Serial synchronous and asynchronous. RS-232, RS-422 and RS-485. HDLC, SDLC, Bisync, NRZ, NRZI, Biphase.
Software Interface:	Control Register ID PROM Z16C30
Initialization:	Hardware Reset initializes Z16C30. Software reset through control register also resets Z16C30
Access Modes:	Word I/O Space Byte I/O Space to Transmit/Receive Data Reg. Word in ID Space Vectored interrupt
Wait States:	Depends on access type. 0 wait states are required for ID PROM and IPCR. USC accesses require 2-3 typically [125 nS per wait state]
Interrupt:	Programmable from Z16C30
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface User cable
Dimensions:	Standard Single IndustryPack width and length. 1.8 x 3.9 inches
Construction:	4 Layer Printed Circuit, Through Hole and Surface Mount Components.
Temperature Coefficient:	0.89 W/°C for uniform heat across IP
Test conditions	20°C, typical
Power Requirements	+5 VDC, 340 mA typ +12 VDC, 60 mA typ –12 VDC, 70 mA typ
Environmental	Operating temperature: 0 to 70°C Humidity: 5 - 95% non-condensing Storage temperature: –10 to +85°C